DOCKET NO. 03-LJ-017 (STMI01-03017) **PATENT**
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Suresh Rajgopal, et al.
Serial No.:	10/750,012
Filed:	December 31, 2003
For:	APPARATUS AND METHOD USING HASHING FOR EFFICIENTLY IMPLEMENTING AN IP LOOKUP SOLUTION IN HARDWARE
Group No.:	2465
Examiner:	Bo Hui Alvin Zhu
Confirmation No.:	9337

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

The Applicants request review of the final rejection in the above-identified application. No amendments are being filed with this request. This request is being filed with a Notice of Appeal. The review is requested for the reasons stated below, demonstrating the clear legal and factual deficiency of the rejections of some or all claims.

Claims 1, 3, 5-14, 16 and 18-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,665,297 to *Hariguchi, et al.* ("*Hariguchi*") in view of U.S. Patent No. 6,067,547 to *Douceur* ("*Douceur*") and further in view of U.S. Patent No. 7,194,740 to *Frank et al.* ("*Frank*"). Claims 2 and 15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hariguchi in view of Douceur and further in view of U.S. Patent No. 5,784,699 to *McMahon, et al.* ("*McMahon*"). Claims 4 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Hariguchi* in view of U.S. Patent Publication No. 2001/0027479 to *Delaney, et al.* ("*Delaney*") and further in view of U.S. Patent No. 6,625,612 to *Tal, et al.* ("*Tal*").

Independent Claim 1 recites an address lookup structure that includes:

> a plurality of hash tables each storing prefixes for address lookups;
> a content addressable memory storing at least some prefixes for which a collision occurs within at least one of the hash tables; and
> a hashing lookup search mechanism that comprises:
> a routing table implemented with selective hashing for a plurality of prefixes with different lengths; and
> a plurality of memory blocks, wherein each hash table is allocated a group of the memory blocks based on a size of the respective hash table and a pre-assigned maximum number of allocated blocks.

The *Hariguchi*, *Douceur*, and *Frank* references, taken alone or in combination, do not teach or suggest each and every element recited in Claim 1. In particular, *Frank* does not provide a disclosure that remedies the conceded deficiencies of *Hariguchi* and *Douceur*. Accordingly, without conceding the propriety of the asserted combination, the asserted combination is likewise deficient.

The Examiner concedes that *Hariguchi* does not teach "each hash table is allocated a group

of the memory blocks based on a size of the respective hash table and a pre-assigned maximum number of allocated blocks." Instead, the Examiner rejects Claim 1 contending that *Douceur* teaches "a hash table is allocated a group of memory blocks based on a size of the respective hash table" and that *Frank* teaches "allocating memory based on a pre-assigned maximum number of memory." (*Office Action*, page 3).

The Examiner asserts that *Frank* (col. 5, lines 31-34) teaches "allocating memory based on a pre-assigned maximum number of memory." However, the Examiner's characterizations of *Frank* are factually incorrect for a number of reasons.

First, *Frank* simply discloses a system to provide a requested memory to a requesting process. *(Frank, Abstract). Frank* discloses that memory has a maximum size and, as such, processes also are limited to a maximum size. *(Frank, col. 1, lines 16-24).* The portion of *Frank* cited by the Examiner only teaches that the process already has a maximum value. *(Frank, col. 5, lines 26-43). Frank* contains no teaching or suggestion that groups of memory blocks are allocated based on a pre-assigned maximum number of allocated blocks. The "pre-assigned maximum number" that the Examiner alleges to be taught in *Frank* is simply a memory limit that is based on the size of the computer system's memory address bus. This is not a "pre-assigned maximum number." There is no "assignment" that occurs that imposes this limit; the limit is simply a function of the size of the computer system's memory address bus. Therefore, *Frank* cannot reasonably be interpreted as teaching or suggesting "wherein each hash table is allocated a group of the memory blocks based on ... a pre-assigned maximum number of allocated blocks."

Second, even if *Frank* could reasonably be construed to teach or suggest a "pre-assigned maximum number" (and the Applicants do not agree that it can be so construed), the memory allocation disclosed in *Frank* is not in any way related to a hash table. *Frank* simply discloses a virtual memory allocation technique that provides a requested memory to a requesting process. *Frank* does not mention hash tables or teach or suggest that any of its disclosed techniques could be used in connection with hash tables. A person of skill in the art would have no reason or motivation to look to any teaching in *Frank* to cure the deficiencies of *Hariguchi* and *Douceur*.

Furthermore, Claim 1 recites that each hash table is allocated a group of memory blocks based on a size of the respective hash table AND a pre-assigned maximum number of allocated blocks. Thus, Claim 1 recites an allocation based on both of two different elements: (i) a size of the respective hash table, and (ii) a pre-assigned maximum number of allocated blocks. Even if *Frank* could reasonably be construed to teach "allocating memory based on a pre-assigned maximum number of allocated blocks", that teaches an allocation based on only one element. Neither *Frank* nor *Douceur* teaches an allocation based on the two different elements recited in Claim 1, and the two references cannot just be combined to render this two-element requirement as obvious.

For at least these reasons, Claim 1 is patentable over *Hariguchi*, *Douceur*, and *Frank*, separately or in combination, and the rejection of Claim 1 over these references is legally and factually deficient.

Independent Claims 10 and 14 recite features analogous to those recited in Claim 1. As such, Claims 10 and 14 are also patentable over *Hariguchi*, *Douceur*, and *Frank*, separately or in

combination, and the rejection of these claims over these references is legally and factually deficient.

The other claims depend from the independent claims and are patentable at a minimum due to their dependence from allowable base claims.

For at least these reasons, the Applicants assert that the claims in the application are in condition for allowance and that the rejections of the claims are both factually and legally deficient. The Applicants respectfully request that this case be returned to the Examiner for allowance or, alternatively, further examination.

The Commissioner is hereby authorized to charge any fees connected with this communication (including any extension of time fees) or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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